Priority Encoder Based Single Cycle Access Structure for Logic Test

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ABSTRACT

In single cycle access test structure for logic test eliminates the power consumption problem of conventional shift-based scan chains and reduces the activity during shift and capture cycles. But it had more complicated in instruction like floating point and it need maximum area. So we propose a priority encoder in the single cycle access test structure to speed up the execution process and reduce the peak power consumption problems.

Keywords— **Low-power testing, Test power reduction, Test-time reduction, Test area reduction.**

I. INTRODUCTION

The common method for delivering test data from chip inputs to internal circuits under test and observing their outputs is called scan-design. In scan-design, registers (flip-flops or latches) in the design are connected in one or more scan chains, which are used to gain access to the nodes of the chip. Test patterns are shifted through the scan chains, functional clock signals are pulsed to test the circuit during the capture cycles and the results are then shifted out to chip output pins and compared against the expected good machine results.

A static compaction procedure for full scan circuits was described to reduce the test application time and optimizing the test pattern. Pomeranz *et al.* [1] it can substantially reduce test application time and power consumption for scan-based testing simultaneously. The test generation method can generate the test set in which the similarity between consecutive bits is significantly higher Chen *et al.* [2] combine different pattern optimization techniques and a clock disabling scheme to further reduce switching activity.

Test pattern optimization to reduce power consumption during test is another aspect. A test pattern generation technique used to minimizing switching activity during scan test by assigning optimized values to don't care bits to limit transactions is shown by Wang *et al.* in [3].

A peak power reduction technique that is based on the dynamic partitioning of the scan chains into multiple groups and inserting delays in the clock tree Almukhaizim *et al.* [4]. The algorithm provides very flexible tools to control the tradeoff between many factors that affect scan test cost and subtrees of the clock to solve the power consumption problem Al-Yamini *et al.* [5]. Reduce power consumption during shift by a multilayer data copy scheme Lin *et al.* [6]. However, most of these methods require a large computational effort and are therefore not applicable for multimillion gate designs or do not simultaneous reduce switching activity and test time. Another critical aspect of SS implementations is at-speed testing.

The high peak power during shift leads to an excessive current due to high switching activity. Ahmed *et al.* in [7] implementing a pipelined global scan enable tree. However, none of the methods fundamentally solve the problem of high switching activity and high number of test cycles and a slow global scan enable signal simultaneously.

The first group uses basically one single address-decoder to select each individual register in the design and an additional element (multiplexer, MUX) per register enables a hold mode of each register. Baik *et al.* [8] a scheme of test pattern generation based on reseeding of segment fixing counter. [9].

The second group addresses each register individually by using an (or row) and a (or column) address decoder with an additional combinatorial element per register cell. The values can be individually read by an additional signal driven by a tristate logic added to each register cell. A modified T-Flip-Flop is shown in [10] to allow the overlap of the test response read out with the loading of the next test input patterns within the same memory addressing cycle. A very similar modified scan register is *l.* in [11] to reduce area overhead of the RAS.

The third group uses a row decoder and a column decoder to address individual registers. Additionally the read/write mechanism is enhanced with two signals per column, driven by a tristate driver, connected to the internal latch cells of the registers via tristate logic and an individual sense amplifier per column.

II. PROPOSED SYSTEN

A novel scan cell register for logic tests combined with a novel scan cell routing architecture. In the structure allows a single cycle access (SCA) to individual register sets. This scheme is fundamentally different to SS. It will compare to a memory with single cycle synchronous write and asynchronous read functionality, whereas the remaining memory content does not change with a certain

number of shift cycles in shift-scan designs, the values are read and written within one single cycle.
It will be shown, that this method can easily be integrated in today's standard flows. The structure needs less test cycles to reach certain or full coverage and the power consumption during tests are in the range of the one in functional mode. This allows higher test frequencies.

III. SCAh-STRUCTURE WITH HOLD MODE

1.SCAh-FF

The single cycle access structure with hold mode (SCAhS) is the signal cycle access register (Flip-Flop, FF) with hold mode (SCAh-FF). It is based on a standard scan register (S-FF) and uses two more priority encoders. The new SCAh-FF can be seen in Figure. 1.
The SCAh-FF has one more input and one more output compared to the standard shift register (S-FF). The inputs clock (clk), data-in (di), and scan-in (si) still exists. The scan-enable is now a 2 bit bus (se[0:1]). An additional scan output pin (so) is added. The reset input and inverse output pins are not shown. The internal logic enables the register to run in one additional hold mode, whereas the additional output priority encoder can bypass the register to directly drive the value of (si). The resulting functionality is best explained by a truth table (see Table I). In functional mode, the register captures (di) and (so) follows (si). In read mode (so) has the value of (do) so that (do) can be read out asynchronously.

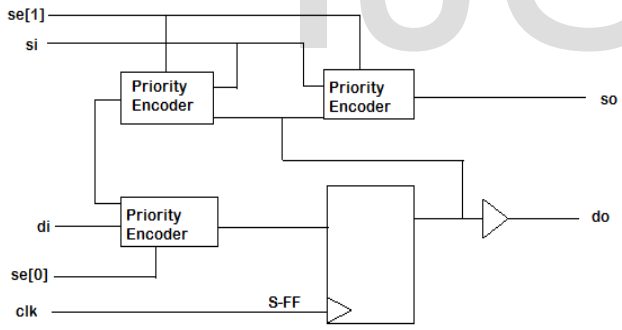

Fig. 1. SCAh-FF based on an S-FF.

TABLE I
TRUTH TABLE OF SCAh-FF

scan enable[0:1]	do@ clk	so	mode
00	di	si	functional
01	di	do	async,
10	do, unchanged	si	hold
11	si	do	sync, write/read

In functional mode, the register captures (di) and (so) follows (si). In read mode (so) has the value of (do) so that (do) can be read out asynchronously. In the event of the relevant clock edge, the register captures (di). In hold mode, (so) follows (si), and the register remains in the state (do), capturing its own value. When, the register captures (si) and (so) changes to the new value of (do) (sync. write/read mode).
The slave latch of a FF is usually connected to the output driver of the data-out pin and/or an inverting driver for the inverse-data-out pin. The internal priority encoder for the SCAh-FF can also be driven by this slave latch output.

2. SCHh-FF Connectivity

Figure 2 shows the SCAh-FF and its connectivity. The two major differences are, that the scan-in (si) is now connected to a dedicated scan-out (so) of the preceding register in the scan chain and the register (se[1]) inputs on the same scan depth are connected to the same line-select (ls) signal, which is driven by a "1 out of N" decoder. In the SCAh-FF connected to the same line-select signal is considered to be on one line. If (add) is 0, no line is selected. (se[0]) of each SCAh-FF is connected to the global scan enable signal (gse). The output of the address decoder is connected to the (se[1]) pin of the registers on one particular line. Additionally, unselected registers remain in hold mode. From this structure four different kinds of cycle modes result.
1) When (gse) is low and (add) is 0, the design works in normal functional mode.
2) If a specific address is given (asynchronous read), the register values on the selected line are passed to the scan-out bus (so). This is called asynchronous read mode.
3) When (gse) is high and (add) is 0 (no line selected), the design remains in hold mode and no register value changes during an clock edge.
4) A specific address is given at a relevant clock edge and (gse) is high, the scan-in values (si) are captured by the registers on the selected line and scan-out (so) is driven by the captured register value (read). This mode is called synchronous write/read.

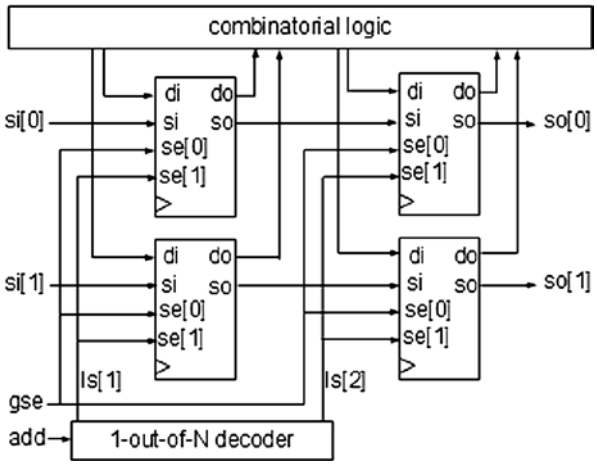

Fig 2. SCAhS connectivity.

3. Peak Power and Power Consumption

The peak power consumption is another serious problem during shift scan. If the data is shifted through the scan chain, the output of the register toggle with a certain

probability. This signal change is then propagated through the adjacent logic. At each clock edge, the power consumption rises to a level, which is much higher than in functional mode.

In SCAhS, the scan-in data and the scan-out data toggle asynchronously through a priority encoder chain and are therefore naturally propagated throughout the complete test cycle. Only a certain number of signals potentially change at a time. The scan data is decoupled from the functional logic. In functional mode, the scan chain does not toggle. It can therefore be assumed, that the peak power is not higher than in functional mode. Therefore impossible to destroy or harm the circuit due to peak power consumption and the circuit behavior is closer to the functional behavior during test. This can be achieved without any major computational effort during pattern optimizations.

The power consumption of a digital sequential circuit can be simplified in the sense, that the power consumption is directly related to the activity on the chip. In order to compare the different power consumptions of the standard shift scan test implementation. The maximum and average activities the SCAhS is compared to the equivalent numbers in function mode and shift-scan-test. A circuit with an SCAhS generates much less activity during stuck-at test than an S-FF-based implementation. If the average or maximum activity is problematic, the test speed can be reduced compared to functional mode or the TS pattern can be optimized.

4. Area

The area of the standard shift (SS) area, each register (FF) is replaced with the corresponding scan FF (S-FF). The two additional pins and the priority encoder result in an area difference of two logic units. If the resulting core area includes a buffered scan-enable tree and a simple XOR-tree for scan-out decompression. The page support area of an SCAh-FF based priority encoder. Additionally one buffer per six registers is added for each line-select signal. If the area for an SCAh-FF is set to 14 logic units. Compared to an S-FF it has two more pins and two more priority encoder, which results in an area difference of three logic units. It does not consider memories, MBIST-logic, power-wells, spare-cells and pad logic.

IV. SCA-STRUCTURE WITHOUT HOLD MODE

1. SCA-FF

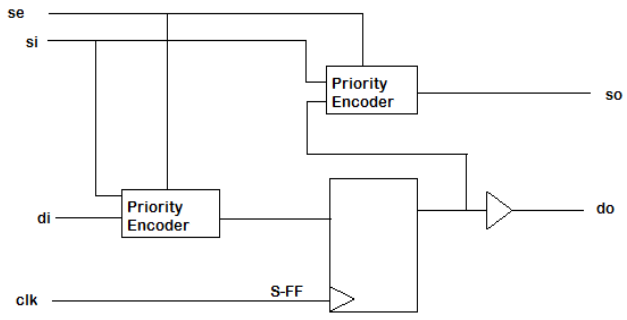

Fig 3. SCA-FF based on an S-FF.

In order to reduce the area overhead of a SCAhS, it adds only one priority encoder to the standard S-FF (see Figure 3). The truth table is shown in Table II. It only has one (se) input, which is connected to the individual line-select signal. The pin is connected to the global enable signal in the SCAhS is removed, so that the complete global scan enable tree becomes obsolete.

TABLE II
TRUTH TABLE OF SCA-FF

scan enable	do@clk	so	mode
0	di	si	functional
1	Si	do	sync, write, async, read

2. Area

The area of a register (FF) is nine logic unit. The corresponding area of a S-FF is 11 logic units and the area of a SCA-FF is set to 13 logic units. The support area "$A_{Support}$" of the SCAS equals the one of a SCAhS without the buffered scan-enable tree. The SCAS area "A_{SCA}" is calculated and the area overhead and compared to a S-FF based implementation.

V. GATED SCA-STRUCTURE

The gated SCAS (gSCAS), which has all the benefits of the SCAhS but only has the area overhead of the SCAS. The hold function of the SCAh-FF is missing in the SCA-FF. It is instead built into the gated clock tree of the gSCAS. Figure 4 shows the connectivity of the gSCA. The scan path reaches from the scan-in AND-selector over the SCA-FF chain and is connected with the input of the XOR-tree.

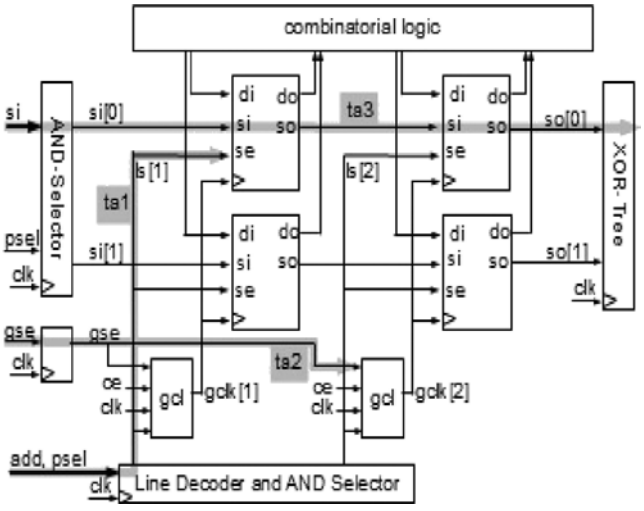

Fig4. gSCAS connectivity.

The individual line-select signals (ls) are connected with the (se) input of the SCA-FF in the relevant line. All SCA-

FF on the lines are clocked by a gated clock element. The gcl is driven by the clock and the line-select signal. The gated clock element can be enhanced, if a clock enable signal (ce) generated by combinatorial logic exists. The global scan enable signal is connected with each gcl, which is already the case in SS if gated clock elements are used to propagate the clock during shift.

TABLE III
TRUTH TABLE OF GATED CLOCK LOGIC

global scan enable	line select	clock enable	gated clk	mode
0	X	0	0	functional disabled
0	X	1	propagate clk	functional enabled
1	0	x	0	hold mode
1	1	x	propagate clk	write mode

The gated clock gcl element's functionality is shown in Table III. If the global scan enable pin (gse) is deselected, the clock is propagated depending on the clock enable signal. In test mode, the clock is only propagated, if the address line is selected. This allows a hold function if (ls) is not selected and a synchronous write if the address line is selected.

1. gSCA—Feasibility, TCPN, Peak Power and Debugging

The "SCAh-Structure with the Hold Mode", we can discussed in various aspects . Most of them are valid for the gSCAS. The insertion of gated clock logic is standard and any existing static timing analysis tool can be used (feasibility). The TCPN number is identical to the one of the SCAhS, because these two implementations of the single cycle access method are functionally identical. Any ATPG algorithm for SS can be used as starting point and the TS is optimized for the single cycle access technique. The problems peak power and the power consumption during tests are eliminated by using the gSCAS.

VI. RUNNING PAGE TESTS IN PARALLEL

A common approach to reduce the TCPN is the method to partition the scan chain into multiple parallel and therefore shorter scan chains [12]. The problem of peak power consumption and high activity during scan shift requires additional enhancements. Especially peak power consumption cannot be eliminated easily in shift-scan based designs. For SCAhS/gSCAS based designs, peak power consumption and activity during test is unproblematic.
The same approach of testing with a higher number of parallel scan chains can be used in single cycle access structures, when multiple pages are enabled at the same time. The write is then done with the same write value to the same line index of each enabled page. The same line is read at each enabled page and the results are then passed through the XOR tree to the output. The activity during the write or read cycles can be adjusted by enabling only an optimal set of pages if it needs to be reduced at all.

VII. RESULTS

The advantage of the single cycle access technique over shift scan-based structures becomes obvious for larger designs. All results listed so far are related to a single scan chain . This is particular useful for the comparison of standard scan implementations and to directly calculate the test amount (TA). The single cycle access structure as well as for the shift based structure will decrease with a higher SW.

VIII. CONCLUSION

Single cycle accesses structure various implementations with and without hold mode as well as gated and partial implementation methods are using priority encoder. The aspects peak power consumption and area. A guide is given how to select the best implementation.
Future work is related to algorithms for reducing the test cycles per net , register reordering, pattern optimization for activity reduction and de-/compression methods for BIST using the gSCAS.

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